



Sheet 1 of 3

<b>Form PTO-1449 Modified</b> <b>List of Patents and Publications Cited by Applicant (Use several sheets if necessary)</b> <b>U.S. Patent Department of Commerce Patent and Trademark Office</b>		<b>Docket No.:</b> 20661-801D1	<b>Serial No.:</b> 09/964,192
		<b>Applicants:</b> Varun Singh, et al.	<b>COPY OF PAPERS ORIGINALLY FILED</b>
		<b>Filing Date:</b> 9/26/01	<b>Group:</b> 2812

**U.S. PATENT DOCUMENTS**

Examiner Initial		Document No.	Date	Name	Class	Subclass
EL	A-1	4,210,996	7/08/1980	Amemiya et al.	29	610
EL	A-2	5,187,559	2/16/1993	Isobe et al.	257	538
EL	A-3	5,854,103	12/29/1998	Liang	438	238
GL	A-4	6,204,105	3/20/2001	Jung	438	238

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**FOREIGN PATENT DOCUMENTS**

Examiner Initial		Document No.	Date	Country	Translation	
					Yes	No
	B-1					



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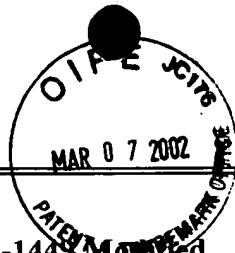
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**OTHER DOCUMENTS**

Examiner Initials		Author, Title, Date, Pertinent Pages, Etc.
YL	C-1	"Electrical Trimming of Heavily Doped Polycrystalline Silicon Resistors", by Yoshihito Amemiya, Terukazu Ono and Kotaro Kato, IEEE Transactions on Electron Devices, Vol. ED-26, No. 11, November 1979
EL	C-2	"A Physical Mechanism of Current-Induced Resistance Decrease in Heavily Doped Polysilicon Resistors", by Kotaro Kato, Terukazu Ono, and Yoshihito Amemiya, IEEE Transactions on Electron Devices, Vol. ED-29, No. 8, August 1982
EL	C-3	"A Monolithic 14 Bit D/A Converter Fabricated with a New Trimming Technique (DOT)", by Kotaro Kato, Terukazu Ono, and Yoshihito Amemiya, IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, October 1984
EL	C-4	"Polysilicon Resistor Trimming for Packaged Integrated Circuits", by J.A. Babcock, D.W. Feldbaumer, and V.M. Mercier, IEEE, 1993
EL	C-5	"Electrical Trimming of Ion-Beam-Sputtered Polysilicon Resistors by High Current Pulses", by Soumen Das and Samir K. Lahiri, IEEE Transactions on Electron Devices, Vol. 41, No. 8, August 1994
EL	C-6	"Constant Voltage Trimming of Heavily Doped Polysilicon Resistors", by Kotaro Kato and Terukazu Ono, Jpn. J. Appl. Phys. Vol. 34, pp. 48-53, January 1995
EL	C-7	"Theory and Application of Polysilicon Resistor Trimming", by D.W. Feldbaumer and J.A. Babcock, Solid-State Electronics Vol. 38, No. 11, pp. 1861 - 1869, 1995
EL	C-8	"Pulse Current Trimming of Polysilicon Resistors", by David W. Feldbaumer, Jeffrey A. Babcock, Vickie M. Mercier, and Christopher K.Y. Chun, IEEE Transactions on Electron Devices, Vol. 42, No. 4, April 1995
EL	C-9	"Change in Temperature Coefficient of Resistance of Heavily Doped Polysilicon Resistors Caused by Electrical Trimming", by Kotaro Kato and Terukazu Ono, Jpn. J. Appl. Phys. Vol. 35, pp. 4209-4215, August 1996
EL	C-10	"Polycrystalline Silicon for Integrated Circuits and Displays Second Edition", by Ted Kamins, P. 266, 1998

Form PTO-144  
PATENT AND TRADEMARK OFFICE**List of Patents and Publications  
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(Use several sheets if necessary)****U.S. Patent Department of Commerce  
Patent and Trademark Office****Docket No.:**  
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6/12/02

**Examiner:**